

JEDEC STANDARD

Marking, Symbols, and Labels for Identification of Lead (Pb) Free Assemblies, Components, and Devices

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MARKING, SYMBOLS AND LABELS FOR IDENTIFICATION OF LEAD (Pb) FREE ASSEMBLIES, COMPONENTS AND DEVICES

Foreword

Certain electronic components and systems are required to be lead (Pb) free as one element of the conditions for meeting the 'Restriction of Hazardous Substances' (RoHS) European directive by July 2006.. There are certain product and solder exemptions to the RoHS legislation that allow the continued use of lead (Pb) thus complicating this standard. As a result there are several lead-free alloys and materials being promoted for the various soldering operations in electronics. Each of these alloys may require different process parameters, including temperatures for manufacturing, assembly, and rework. Some means of communicating the identity of the lead-free material must be provided so that those performing assembly, rework, and recycling operations are aware of the capabilities and limitations of these materials. The requirements set forth in this standard are considered minimal and additional information may be supplied using other labels or marking schemes.

MARKING, SYMBOLS AND LABELS FOR IDENTIFICATION OF LEAD (Pb) FREE ASSEMBLIES, COMPONENTS AND DEVICES

(From JEDEC Board Ballot JCB-04-41, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices and the JC-14.4 Subcommittee on Quality Processes and Methods.)

1 Scope

This document shall apply to all electronic components including passives, connectors, solid state components and other devices which use solder to attach the device/component to the board or assembly. This standard applies to bumped die that are used for direct board attach (COB). This standard presumes that the surface finish of bare boards (PCB), package substrates, etc. is Pb-free.

NOTE The Pb-free labeling of electronic systems, such as computers, printers, servers, etc, is outside the scope of this standard.

The purpose of this publication is to provide a distinctive symbol and labeling format to identify those assemblies, components or devices that are totally Pb-free and/or are capable of providing or have Pb-free 2nd level interconnects. It also provides for identification of certain types of Pb-free materials and the maximum safe processing temperature during assembly or rework. It is meant to address only the Pb-free aspects RoHS compliance and does not address compliance to other banned materials.

2 Normative reference

Directive 2002/95/EC of the European Parliament and of the Council on the *Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment* ("RoHS Directive"). The exemptions are listed in an Annex of this directive.

3 Terms and definitions

3.1 2nd level interconnect: The interconnect made by the attachment of the device/component to the printed circuit board, see Figure 5.

3.2 2nd level interconnect label: A label that identifies boxes, bags or containers that contain boards/assemblies or components capable of or that have Pb-free 2nd level interconnects.

NOTE This label includes the Pb-free category and maximum processing temperature, see Figure 4.

3.3 bar code label: A label that gives information in a code consisting of parallel bars and spaces, each of various specific widths.

NOTE For the purposes of this standard, the bar code label is on the lowest level shipping container and includes information that describes the product, e.g., part number, quantity, lot information, supplier identification, moisture-sensitivity level, etc.

3 Terms and definitions (cont'd)

3.4 intct: Abbreviation for the word “interconnect”.

3.5 Pb-free (lead-free): Electrical and electronic assemblies and components in which the Lead (Pb) level in any of the raw materials and the end product is less than or equal to 0.1% by weight and also meets any Pb-free requirements/definitions adopted by the ROHS Directive 2002/95/EC.

NOTE: A 'Pb-free' component may not necessarily be compatible with Pb-free processing temperatures, as process-compatibility must be determined by the "maximum safe temperature" (see 4.4.1).

3.6 Pb-free category: A category assigned to Pb-free components, boards, and assemblies indicating the general family of material used for the 2nd level interconnect including solder paste, lead/terminal finish, and terminal material/alloy solder balls.

3.7 Pb-free identification label: A label that indicates that the enclosed components, devices, and/or board assemblies are considered to be Pb-free, (i.e., Pb-free as defined in 3.5).

NOTE It is not to be applied to items that contain Pb but are exempt according to the RoHS directive, see Figure 3.

3.8 Pb-free symbol: A symbol that can be used in place of the phrase “Pb-free”, see Figure 2.

3.9 RoHS: Acronym for European Directive, *Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment*.

4 Symbols and labels

4.1 Pb-free category symbol

This symbol (see figure 1) is used to identify the 2nd level interconnect material defined in 5. It is to be marked on components, devices, and assemblies.

4.1.1 Size

The size and location of the mark shall be optional but be legible to corrected, unmagnified vision.

4.1.2 Color

The color for the ‘e’ and category number should be selected to provide sufficient contrast to be legible to corrected, unmagnified vision.

4 Symbols and labels (cont'd)

4.1.3 Font

The font style should be “Arial”, “OCR-A” or equivalent.



Figure 1 — Example of mark showing category 2 and option of circle or ellipse

4.2 Pb-free symbol

This symbol (see figure 2) can be used as an option to replace the phrase “Pb-free” on labels or wherever practical on components/devices, boards, assemblies etc.



Figure 2 — Pb-free Symbol

4.3 Pb-free identification label

This label (see figure 3) shall only be used when the components/devices and/or board assemblies are totally Pb-free, according to the definition given in 3.5 and should be affixed to intermediate boxes, or other containers that are not otherwise identified as Pb-free.

NOTE Items that contain Pb shall not use this label even if exempted by RoHS.

4.3.1 Size

It is recommended the label be a minimum of 22 mm x 25 mm with the minimum diameter of the circle being 18 mm.

4.3.2 Color

The background shall be white and the symbol and letters shall be of a contrasting color. The color Red should be avoided as red suggests a personal hazard.

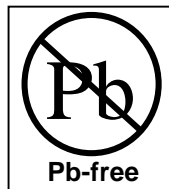


Figure 3 — Pb-free Identification Label

4 Symbols and labels (cont'd)

4.4 2nd level interconnect label

This label (see figure 4) indicates that the 2nd level interconnect terminal finish/material of components and/or the solder paste/solder used in board assembly are Pb-free. The categories are defined in 5. This label shall be placed/printed on the lowest level shipping container and any “ESD”, “Dry pack” or other bag/box, excluding tubes, trays, reels or other carriers, within the lowest level shipping container.

The use of the 2nd level interconnect label is optional if the following information is included on the bar code or other nearby label, in human readable form: 1) the “Pb-free” symbol, or the words “Pb-free” and/or, 2) the words “2nd level interconnect”, 3) The category, and 4) the maximum safe operating temperature. If the enclosed component/devices or assemblies are totally Pb-free then the words “2nd level interconnect” may be omitted and/or replaced by the Pb-free symbol or the words “Pb-free” on the labels.

NOTE 1 If the category is used without the circle/ellipse it must be made clear that the marking defines the category, [e.g., Category = e2 or Category = (e2) or Pb-free (e2)]. Parenthesis may be used in place of the circle/ellipse if using printers without graphic capability.

NOTE 2 If the label size/area prevents printing the words “2nd level interconnect” They may be abbreviated as long as the meaning is clear, e.g. “2nd lvl intct”.

4.4.1 Components

If the label is affixed to containers holding components/devices, the category field shall describe the terminal finish/material. The “maximum safe temperature” field shall indicate the maximum temperature the component/device should obtain during assembly.

4.4.2 Assemblies

If the label is affixed to containers holding boards/assemblies, the category field shall describe the solder paste/solder used in the board assembly and the “maximum safe temperature” field shall contain the maximum safe processing temperature of the board and components.

4.4.3 Size

It is recommended that the Pb-free label be a minimum of 75 mm by 50 mm.

4.4.4 Color

The label shall be black letters/symbols on a white or contrasting background.

NOTE Since the European legislation, RoHS, allows for exemptions of Pb content in certain applications, the Pb-free symbol on this label indicates that the material has Pb-free 2nd level interconnects only, it does not indicate that the component/devices or assemblies are totally Pb-free.

4 Symbols and labels (cont'd)

4.4 2nd level interconnect label (cont'd)

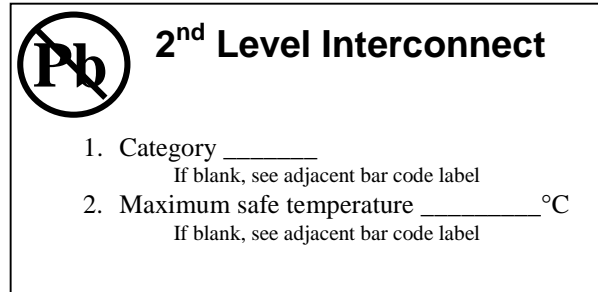


Figure 4 — 2nd Level interconnect label

Table 1 gives a summary of how these symbols and labels are used on components and board assemblies.

Table 1 — Pb-free marking & labeling summary

Item	Mark location	Marking requirements		Ref Clause
		Required	Optional	
Component	- Top of package	- Pb-free category for component terminal finish/material– If space permits	Pb-free symbol for components Pb-free per 3.5	6
Component Packing - Lowest level shipping container	- Can be on bar code label or 2 nd level interconnect label	- Pb-free category for component terminal finish/material - Maximum safe processing temperature for component	Pb-free symbol/label for components Pb-free per 3.5	6
Component Packing - Dry Pack/ESD or other Bag if used	- Can be on bar code label or 2 nd level interconnect label	- Pb-free category for component terminal finish/material - Maximum safe processing temperature for component	Pb-free symbol/label for components Pb-free per 3.5	6
PCB Assemblies	- Topside, lower right-hand segment	- Pb-free category for assembly solder type(s) - Maximum safe processing temperature	Pb-free symbol/label for assemblies Pb-free per 3.5	7 7.2
Assemblies Packing		- Pb-free category for assembly solder type(s) - Maximum safe processing temperature	Pb-free symbol/label for assemblies Pb-free per 3.5	7
Bare PCB Board		None required, surface finish shall be Pb-free		1.2

5 Pb-Free categories

The following categories are meant to describe the Pb-free 2nd level interconnect (see figure 1) terminal finish/material of components and/or the solder paste/solder used in board assembly.

- e1 - SnAgCu (shall not be included in category e2)
- e2 - Sn alloys with no Bi or Zn excluding SnAgCu
- e3 - Sn
- e4 - Precious metal (e.g., Ag, Au, NiPd, NiPdAu) (no Sn)
- e5 - SnZn, SnZnx (no Bi)
- e6 - contains Bi
- e7 - low temperature solder (≤ 150 °C) containing Indium (no Bi)

e0, e8, e9 symbols are unassigned at this time.

6 Component marking

On a component with normal marking, if space permits, the individual device/component shall be marked with the category designation enclosed within a circle/ellipse, see Figure 1.

If the category and maximum safe temperature is marked on the component and the lowest level shipping container then no other Pb-free symbols or labels are required on the shipping containers.

If the individual component cannot be marked, the category shall be indicated on the lowest level shipping container utilizing the “2nd level interconnect label” (see Figure 4) and/or a nearby label see 4.4.

If the label is affixed to containers holding components/devices, the category field shall describe the terminal finish/material and the “maximum safe temperature” indicating the maximum temperature the component/device should obtain during assembly.

If the components are considered Pb-free according, to 3.5 then the Pb-free label (Figure 3) may be utilized on the containers and/or the Pb-free symbol (Figure 2) may be used on the components or labels without the words “2nd level interconnect” following the symbol.

7 Board/assembly marking

This standard presumes that the bare board (PCB) surface finish is Pb-free. Boards/assemblies will be identified as being assembled with Pb-free solders and using components with Pb-free 2nd level interconnect leads/terminals by marking using the words “Pb-free 2nd level interconnect” or the Pb-free symbol shown in figure 2 followed by the words “2nd level interconnect”.

If the Boards/assemblies are considered Pb-free according to 3.5 then the words “2nd level interconnect” may be omitted after the words “Pb-free” or the Pb-free symbol. In addition the category (with or without the circle), as defined in 5 and the maximum safe processing temperature will be shown on the board/assembly.

7 Board/assembly marking (cont'd)

If either the category or the maximum safe processing temperature cannot or are not placed on the board/assembly then the 2nd level interconnect label (see figure 4) shall be utilized on the lowest level shipping container.

If the label is affixed to containers holding boards/assemblies, the category field shall describe the solder paste/solder used in the board assembly. If the “maximum safe temperature” field is blank, then 260 °C is assumed.

If the boards/assemblies are considered Pb-free according to 3.5 then the Pb-free label may be utilized on the containers and/or the Pb-free symbol may be used on the boards/assemblies or labels without the words “2nd level interconnect” following the symbol.

NOTE If the category is used without the circle/ellipse it must be made clear that the marking defines the category, [e.g., Category = e2 or Category = e2 or 2nd level interconnect = (e2), etc.]. If using printers without graphic capability, parenthesis may be used in place of the circle/ellipse.

7.1 Category hierarchy

If two or more solder alloys are used (e.g., Reflow and wave solder use different category solder alloys) the category of the reflow(s) will be shown first and the wave solder category will follow.

7.2 Location

The preferred location for marking of the categories is on PCB layer 1 (topside) at the lower right-hand segment.

7.3 Size

The size of the mark is optional but shall be legible to corrected, unmagnified vision.

7.4 Color

The color for the ‘e’ and category number shall be selected to provide sufficient contrast to be legible to corrected, unmagnified vision.

7.5 Font

The font style should be “Arial”, “OCR-A” or equivalent.

7.6 Method

The methods, e.g., screen print, etch, laser etc., for marking of the board is optional but it shall be legible to corrected, unmagnified vision.

7 Board/assembly marking (cont'd)

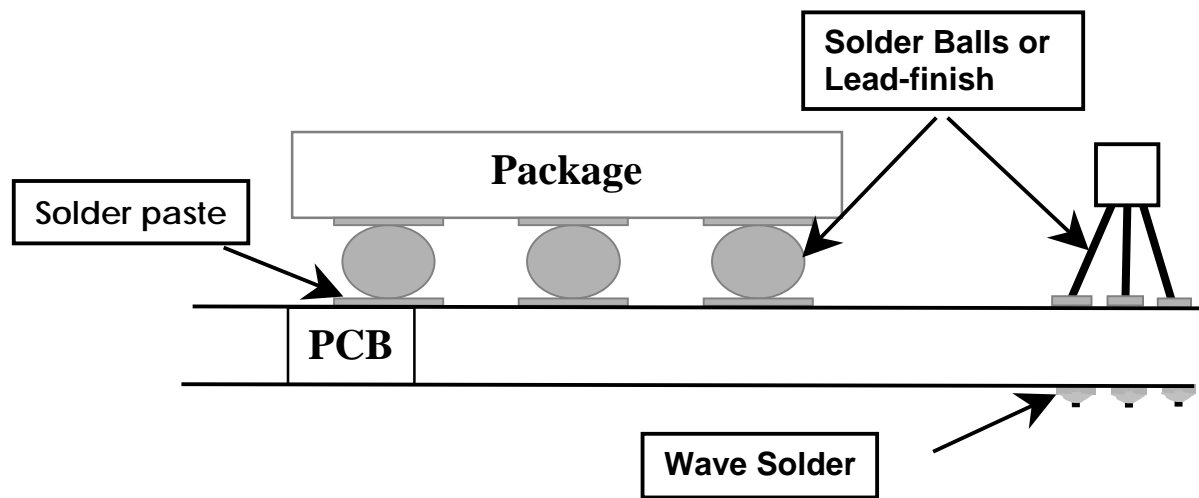


Figure 5 — 2nd level interconnect



Standard Improvement Form

JEDEC JESD97

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

Requirement, clause number _____

Test method number _____ Clause number _____

The referenced clause number has proven to be:

Unclear Too Rigid In Error

Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by

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Phone: _____

Company: _____

E-mail: _____

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